ABSTRACT

Described are small, efficient SRAM cells that are insensitive to read errors. SRAM cells in accordance with one embodiment include a pair of cross-coupled inverters extending between first and second bit nodes and a read amplifier extending from one of the first and second bit nodes to an associated bitline. During a read access to a given memory cell, the corresponding read amplifier isolates the bit nodes from the bitlines to prevent the voltage on bitline BL from disturbing data stored in the memory cell.